Also on page 9, line 26, please replace "silane oxynitride" with -- silane-based oxynitride --.

On page 9, line 29, please replace "silane" with -- silane-based --.

On page 9, line 30, please replace "silane oxide" with -- silane-based oxide --.

IN THE CLAIMS

Please amend the claims as follows.

Please cancel claims 1-35 without prejudice.

Please add the following claims:

a2

36. A semiconductor device, comprising:

an electrically conductive member;

a dielectric layer under said conductive member, said dielectric layer containing a dopant and a contaminant;

a contaminant barrier under said dielectric layer;

an insulating region under said contaminant barrier; and

a plurality of electrically conductive regions under said contaminant barrier and flanking said insulating region.

37. The semiconductor device in claim 36, wherein said contaminant barrier comprises at least one material selected from an oxide, an oxynitride, a nitride, and combinations thereof.

38. The semiconductor device in claim 37, wherein said contaminant barrier comprises at least two materials selected from an oxide, an oxynitride, a nitride, and combinations thereof.

39. The semiconductor device in claim 37, wherein said electrically conductive member comprises a lead.

A2 Cont'd.

40. A circuit device, comprising:

a conductive structure configured to receive a voltage;

a first insulation portion under said conductive structure, said first insulation portion including an organic contaminant;

a second insulation portion under said first insulation portion, said second insulation portion having an index of refraction ranging from 1.5 to 2.6; and

a substrate under said second insulation portion and comprising:

an electrically conductive first region,

an electrically conductive second region, and

an insulation region between said first region and said second region.

41. The circuit device in claim 40, wherein said first region is a first active area within a well; and said second region is a second active area within said well.

42. The circuit device in claim 40, wherein said first region is a first well and said second region is a second well.

43. The circuit device in claim 40, wherein said first region is a first n-well and said second region is a second n-well.

44. An insulative stack between a top conductive member and a lower-lying plurality of conductive areas, said insulative stack comprising:

an insulating region between said plurality of conductive areas;

a carbon barrier over said insulating region; and

a carbon-containing dielectric over said carbon barrier and under said top conductive member.

45. The insulative stack in claim 44, wherein said insulating region comprises a field oxide.

46. The insulative stack in claim 44, wherein said insulating region comprises a trench oxide.

A² Contd.

47. A barrier between a dielectric contaminated with an electrically chargeable material and an insulating region generally free of said electrically chargeable material, said barrier comprising insulation for an integrated circuit device, wherein said insulation defines a first interface with said dielectric and a second interface with said insulating region; and wherein said first interface has a first concentration of said electrically chargeable material that is greater than a second concentration of said electrically chargeable material at said second interface.

48. The barrier in claim 47, wherein said insulation comprises aluminum oxide.

49. The barrier in claim 47, wherein said insulation comprises aluminum nitride.

50. The barrier in claim 47, wherein said insulation has a thickness ranging from 50 Angstroms to 2000 Angstroms.

51. The barrier in claim 50, wherein said insulation has a thickness ranging from 100 Angstroms to 1000 Angstroms.

52. A method of processing a semiconductor device, comprising:

depositing a dielectric layer over a semiconductor substrate;

allowing electrically chargeable particles to occur in said dielectric layer;

allowing some diffusion of said electrically chargeable particles; and

preventing at least some of said electrically chargeable particles from reaching said substrate.

53. The method in claim 52, wherein:

said step of depositing a dielectric layer comprises depositing a dielectric layer using a organic precursor;

said step of allowing electrically chargeable particles to occur in said dielectric layer comprises allowing an organic component of said organic precursor to deposit in said dielectric layer; and

said preventing step comprises layering a barrier over said substrate using a non-organic precursor prior to said step of depositing a dielectric layer.

54. The method in claim 53, wherein said layering step comprises layering a barrier using silane.

55. A method of at least partially forming a circuit device, comprising:

providing a semiconductor substrate;

layering a carbon-free barrier on said substrate; and

layering a carbon-containing dielectric on said barrier.

56. The method in claim 55, wherein said step of layering a carbon-free barrier on said substrate further comprises layering said carbon-free barrier using a plasma.

57. The method in claim 56, further comprising a step of heating said carbon-containing dielectric.

58. The method in claim 57, wherein said step of heating said carbon-containing dielectric comprises raising a temperature of said dielectric to a range of 850° C to 1050° C for at least 5 seconds.

59. The method in claim 57, wherein said step of heating said carbon-containing dielectric comprises raising a temperature of said dielectric to a range of 750° C to 1000° C for at least 5 minutes.

60. A method of processing a substrate comprising two active areas and an intervening insulating region, said method comprising:

depositing an oxide charge barrier over said substrate;

depositing a generally insulative material over said oxide charge barrier, wherein said generally insulative material is less insulative than said barrier; and

providing a generally conductive element over said generally insulative material,